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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

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EXAMINER
THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/273,560	Applicant(s) HASEGAWA, TAKUMI	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *14 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Introduction

1. Claims 1 to 4 of the Application 09/273560 filed on 22 March 1999 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** (U.S. Patent 5,274,568) in view of **Hasegawa (HS)** (U.S. Patent 5,528,511).

As per Claim 1, **BL** recites the delay analysis system for delay analysis of a logic circuit. (See Col 1, Lines 7-9)

BL also teaches a delay analysis library. (See Col 1, Lines 9-13)

BL also teaches the library containing connection information on a plurality of circuits. (Col 1, Lines 39-40)

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal. (Col 1, Lines 45-48)

BL does not appear to teach the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of plurality of circuits. **BL** also does not appear to teach that when making a delay analysis of the logic circuit including

at least one of plurality of circuits, a delay time is selected from the delay time information according to a logical operation of one of the circuits.

HS teaches that the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of plurality of circuits. (Figs. 3, 6 and 8 and Col 3, Lines 5-26). **HS** also teaches that when making a delay analysis of the logic circuit including at least one of the plurality of circuits, a delay time is selected from the delay time information according to a logical operation of one of the circuits. (Col 3, Lines 5-26).

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the logical information storage and application to modify the delay time computation of **HS** in order to compute the delay times more accurately in logical circuits involving combinatorial operations.

4. As per Claim 2, **BL** recites the delay analysis system for delay analysis of a logic circuit. (See Col 1, Lines 7-9)

BL also teaches a delay analysis library. (See Col 1, Lines 9-13)

BL also teaches the library containing connection information on a plurality of circuits. (Col 1, Lines 39-40)

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal. (Col 1, Lines 45-48)

BL does not appear to teach the library further contains logical operation information representing correspondence between a logical value of each input terminal

and the logical value of the output terminal of at least one of plurality of circuits. **BL** also does not appear to teach that when making a delay analysis of a logic circuit, a delay time between the input terminal and the output terminal is selected from the delay time information according to a logical operation of the circuit.

HS teaches that the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of plurality of circuits. (Figs. 3, 6 and 8 and Col 3, Lines 5-26). **HS** also teaches that when making a delay analysis of a logic circuit, a delay time between the input terminal and the output terminal is selected from the delay time information according to a logical operation of the circuit. (Col 3, Lines 5-26).

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the logical information storage and application to modify the delay time computation of **HS** in order to compute the delay times more accurately in logical circuits involving combinatorial operations.

5. As per Claim 1, **BL** recites a method for making a delay analysis of a logic circuit. (See Col 1, Lines 7-9)

BL also teaches referencing a delay analysis library. (See Col 1, Lines 9-13)

BL also teaches the library containing connection information on a plurality of circuits. (Col 1, Lines 39-40)

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal. (Col 1, Lines 45-48)

BL does not appear to teach the library contains logical operation information representing correspondence between a logical value of each input terminal and a logical value of the output terminal of at least one of plurality of circuits. **BL** also does not appear to teach selecting the delay time of at least one of circuits from delay time information according to a specified logical operation of the circuit.

HS teaches that the library further contains logical operation information representing correspondence between a logical value of each input terminal and a logical value of the output terminal of at least one of plurality of circuits. (Figs. 3, 6 and 8 and Col 3, Lines 5-26). **HS** also teaches selecting the delay time of at least one of circuits from the delay time information according to a specified logical operation of the circuit. (Col 3, Lines 5-26).

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** with the logical information storage and application to modify the delay time computation of **HS** in order to compute the delay times more accurately in logical circuits involving combinatorial operations.

6. As per Claim 4, **BL** teaches referencing a delay analysis library. (See Col 1, Lines 9-13)

BL also teaches the library containing connection information on a plurality of circuits. (Col 1, Lines 39-40)

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal. (Col 1, Lines 45-48)

BL does not appear to teach the library contains logical operation information representing correspondence between a logical value of each input terminal and a logical value of the output terminal of at least one of plurality of circuits. **BL** also does not appear to teach selecting the delay time of at least one of circuits from delay time information according to a specified logical operation of the circuit. **BL** also does not appear to teach a computer readable medium having stored thereon a program for executing a process step for referencing a delay analysis library and selecting the delay time. **BL** also does not appear to teach a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one of circuits.

HS teaches the library contains logical operation information representing correspondence between a logical value of each input terminal and a logical value of the output terminal of at least one of plurality of circuits. (Figs. 3, 6 and 8 and Col 3, Lines 5-26). **HS** also teaches selecting the delay time of at least one of circuits from delay time information according to a specified logical operation of the circuit. (Fig. 9 and Col 3, Lines 5-26). **HS** teaches a delay time verification unit. (Col 2, Lines 61-62). It is understood that the verifier unit has a computer readable medium having stored thereon a program for executing the method for delay analysis. So **HS** also teaches a computer readable medium having stored thereon a program for executing a process step for referencing a delay analysis library and selecting the delay time. **HS** also teaches a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one of circuits. (Fig. 9 and Col 3, Lines 5-26).

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the computer readable medium having stored thereon a program for computing modified delay times using the logical information storage and application of **HS** in order to compute the delay times more accurately in logical circuits involving combinatorial operations.

Response to Arguments

7. Applicant's arguments, filed on 1/14/02 have been carefully considered and are not persuasive.

8. Claim rejection under 35 U.S.C. 112 first paragraph is withdrawn in response to arguments.

9. Applicant's arguments regarding art rejections are moot in view of the new rejections which are applied against the amended claims.

ACTION IS FINAL, NECESSIATED BY AMENDMENT

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DR. HUGH M. JONES
PATENT EXAMINER
ART UNIT 2123

K. Thangavelu
Art Unit 2123
February 27, 2002